IN THE CLAIMS

Please amend the claims as follows.

1-26. (Cancelled).

27. (Currently Amended) A gate stack, comprising:

a gate oxide layer over a semiconductive substrate;

a polysilicon layer on the gate oxide layer;

~~a~~ an annealed metal silicide layer on the polysilicon layer;

a layer comprising $Si_xN_yO_z$:H formed over and in physical contact with the metal silicide, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33; the annealed metal silicide being the product of a process in which the metal silicide is subjected to an anneal treatment after the layer comprising $Si_xN_yO_z$:H is formed, wherein the layer comprising $Si_xN_yO_z$:H protects the annealed metal silicide layer during the anneal; and

a silicon nitride layer on the layer comprising $Si_xN_yO_z$:H the polysilicon layer, the gate oxide layer, the metal silicide layer, the layer comprising $Si_xN_yO_z$:H, and the silicon nitride layer being patterned to form the gate stack.

28-32. (Cancelled).

33. (Previously presented) The gate stack of Claim 27, where the layer comprising $Si_xN_yO_z$:H has a thickness of from about 250Å to about 650Å.

34-35. (Cancelled).

36. (Previously presented) The gate stack of claim 27 wherein y is from 0.02 to less than 0.1.

37. (Previously presented) The gate stack of claim 27 wherein x = 0.5, y = 0.37 and z = 0.13.

38. (Previously presented) The gate stack of claim 27 wherein the metal silicide layer comprises titanium.

39-43. (Cancelled)

44. (New) A gate stack, comprising:

a gate oxide layer over a semiconductive substrate;

a polysilicon layer on the gate oxide layer;

an annealed, metal silicide layer on the polysilicon layer;

a means for protecting the metal silicide layer during an anneal, the means for protecting consisting of a $Si_xN_yO_z$:H layer formed over and in physical contact with the metal silicide layer, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33, the means for protecting the metal silicide layer being adapted to act as an antireflective layer; and

a silicon nitride layer on the $Si_xN_yO_z$:H layer.

45. (New) The gate stack of claim 44, wherein x = 0.5, y = 0.37 and z = 0.13.

46. (New) The gate stack of claim 44, wherein the metal silicide layer comprises titanium.

47. (New) The gate stack of claim 44, wherein the $Si_xN_yO_z$:H layer has a thickness of from about 250Å to about 650Å.

48. (New) The gate stack of claim 44, wherein the means for protecting the annealed metal silicide layer is adapted to protect the metal silicide layer from gaseous oxygen during the anneal.

49. (New) The gate stack of claim 48, wherein the means for protecting the annealed metal silicide layer is adapted to alleviate stress exerted by the silicon nitride layer on layers underlying the layer comprising $Si_xN_yO_z$:H layer.

50. (New) A gate stack, comprising:

a gate oxide layer over a semiconductive substrate;

a polysilicon layer on the gate oxide layer;

an annealed, titanium silicide layer on the polysilicon layer;

a means for alleviating stress on underlying layers, canceling reflected radiation, and protecting the titanium silicide layer during an anneal from gaseous oxygen, the means comprising a $Si_xN_yO_z$:H layer formed over and in physical contact with the titanium silicide layer, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33; and

a silicon nitride layer on the $Si_xN_yO_z$:H layer.

51. (New) The gate stack of claim 50, wherein $x = 0.5$, $y = 0.37$ and $z = 0.13$.

52. (New) The gate stack of claim 52, wherein the $Si_xN_yO_z$:H layer has a thickness of from about 250Å to about 650Å.